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EXAMINER	
RODRIGUEZ, GLENDA P	

ART UNIT	PAPER NUMBER
2627	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,876	OZDEMIR, HAKAN	
	Examiner	Art Unit	
	Glenda P. Rodriguez	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-57 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-57 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~6/24/05 & 6/16/06~~
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5, 10, 13-15, 17, 18, 22, 23, 29, 31-33, 39-46, 51, 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sacks et al. (US Patent No. 6, 181, 505) in view of Tuttle et al. (Patent No. 6, 108, 151).

Regarding Claims 1 and 38, Sacks et al. teach a servo circuit, comprising:

> A servo channel operable to recover servo data from servo wedges that identify respective data sectors on a data-storage disk (Pat. No. 6, 181, 505; Col. 6, Lines 3-26);
>
> And a processor coupled to and operable to control the servo channel (Pat. No. 6, 181, 505; Col. 6, Lines 3-26).

Sacks et al. fails to teach a processor is operable to detect one of the servo wedges during or after disk spin-up search operation without first detecting a spin-up wedge. However, this feature is well known in the art as disclosed by Tuttle et al., wherein it teaches the detection of the preamble of the servo wedges without first detecting a spin up wedge (Pat. No. 6, 108, 151; Col. 4, L. 29-56 and See also Col. 15, L. 12-43, wherein Tuttle et al. teaches the detection of a servo wedge while the disk is attaining a steady speed. This wedge then provides a location of the head with respect to the disk as taught by Tuttle therein. Applicant cites that "servo wedge" is a portion of the servo sector in which non-application data is stored, as taught in page 2, Lines 5-

10 of Applicant's Specification.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Sacks et al.'s invention to detect one of the servo wedges during or after disk spin-up search operation without first detecting a spin-up wedge in order to synchronize the timing recovery in the servo channel.

Apparatus claim 22 is drawn to the apparatus corresponding to the method of using same as claimed in claim 1 and 38. Therefore apparatus claim 22 corresponds to method claims 1 and 38, and is rejected for the same reasons of obviousness as used above.

Regarding Claim 2 and 23, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claims 1 and 22, respectively. The combination further teach wherein the processor is operable to cause the servo channel to recover servo data from the one servo wedge after the processor detects the one servo wedge and before the servo channel recovers servo data from any other servo wedge (Pat. No. 6, 108, 151; Col. 4, Lines 29-56 Applicant cites that "servo wedge" is a portion of the servo sector in which non-application data is stored, as taught in page 2, Lines 5-10 of Applicant's Specification.).

Regarding Claim 3 and 24, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claims 1 and 22, respectively. The combination further teach the one servo wedge comprises a preamble and the processor is operable to detect the one servo wedge by detecting the preamble (Pat. No. 6, 108, 151; Fig. 2B and Col. 4, Lines 29-56. Applicant cites that "servo wedge" is a portion of the servo sector in which non-application data is stored, as taught in page 2, Lines 5-10 of Applicant's Specification.).

Regarding Claim 4 and 25, the combination of Sacks et al. teach all the limitations of Claims 1 and 22, respectively. The combination further teach the one servo wedge comprises a

preamble and a servo synchronization mark following the preamble; the processor is operable to detect the one servo wedge by detecting the preamble; and the servo channel is operable to recover the synchronization mark in response to the processor detecting the preamble (Pat. No. 6, 108, 151; Fig. 2B and Col. 4, Lines 29-56. Applicant cites that "servo wedge" is a portion of the servo sector in which non-application data is stored, as taught in page 2, Lines 5-10 of Applicant's Specification.).

Regarding Claim 5, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 1. The combination further teach the one servo wedge and a servo wedge following the one servo wedge each comprise a preamble and a servo synchronization mark following the preamble; the processor is operable to detect the one servo wedge by detecting the preamble of the one servo wedge; the servo channel is operable to recover the synchronization mark of the one servo wedge in response to the processor detecting the preamble of the one servo wedge; after detecting the one servo wedge, the processor is operable to detect the following servo wedge by detecting the preamble of the following servo wedge; and the servo channel is operable to recover the synchronization mark of the following servo wedge in response to the processor detecting the preamble of the following servo wedge (Pat. No. 6, 108, 151; Fig. 2B and Col. 4, Lines 29-56. It is obvious to a person of ordinary skill in the art to know that the servo channel during will read more than one servo wedge when the disk is in a spinning operation. Applicant cites that "servo wedge" is a portion of the servo sector in which non-application data is stored, as taught in page 2, Lines 5-10 of Applicant's Specification.).

Regarding Claims 10 and 29, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claims 1 and 22, respectively. The combination further teach: one the one servo

wedge comprises a preamble (Pat. No. 6, 108, 151; Fig. 2B); the servo channel is operable to generate a read signal that represents the servo wedge and to sample the read signal (Col. 4, Lines 57-60. It presents a channel that reads both servo and user data.); the processor is operable to detect the one servo wedge by detecting the preamble from the samples (Col. 4, Lines 47-56); the servo channel comprises an interpolator loop that acquires the timing of the samples with respect to the read signal while the processor is detecting the preamble and that begins tracking the timing of the samples a predetermined time after the processor detects the preamble (Col. 21, Lines 3-31).

Regarding Claims 13 and 31, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 1 and 22, respectively. The combination further teach the one servo wedge comprises a preamble (Pat. No. 6, 108, 151; Fig. 2B); the servo channel is operable to generate a read signal that represents the servo wedge and to sample the read signal; and the processor is operable to detect the preamble if and only if a predetermined number of consecutive samples represent the preamble (Fig. 2, and Col. 4, Lines 47-56. It is obvious to a person of ordinary skill in the art that a preamble has a predetermined number of consecutive samples.).

Regarding Claims 14 and 54, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claims 1 and 38, respectively. The combination further teach wherein the one servo wedge comprises a preamble (Pat. No. 6, 108, 151; Fig. 2B); wherein the servo channel is operable to generate a read signal that represents the servo wedge and to sample the read signal (Col. 4, Lines 57-60. It presents a channel that reads both servo and user data.); wherein the processor is operable to detect the one servo wedge by detecting the preamble from the samples (Pat. No. 6, 108, 151; Col. 4, Lines 47-56); wherein the servo channel comprises an interpolator

loop that acquires the timing of the samples with respect to the read signal while the processor is detecting the preamble and that begins tracking the timing of the samples a predetermined time after the processor detects the preamble and an initial-timing circuit operable to calculate an initial timing difference between the samples and the read signal and to provide an initial timing adjustment to the interpolator loop while the interpolator loop is acquiring the timing of the samples (Pat. No. 6, 108, 151; Col. 21, Line 65 to Col. 22, Line 62).

Regarding Claims 15, 33 and 55, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claims 1, 22 and 38, respectively. The combination further teach wherein the one servo wedge comprises a preamble (Pat. No. 6, 108, 151; Fig. 2B); wherein the servo channel is operable to generate a read signal that represents the servo wedge, to amplify the read signal with a gain, and to sample the read signal; wherein the processor is operable to detect the one servo wedge by detecting the preamble from the samples and an initial-gain circuit operable to calculate an initial amplitude of the read signal and to provide an initial gain adjustment to the servo channel (Col. 21, Lines 45-59).

Regarding Claim 16, 34 and 56, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claims 1, 22 and 38, respectively. The combination further teach wherein the one servo wedge comprises a binary sequence having groups of no more and no fewer than a predetermined number of consecutive bits each having a first logic level, the groups separated from each other by respective bits having a second logic level (Col. 16, Lines 30-67).

Regarding Claims 17 and 35, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claims 1 and 22, respectively. The combination further teach wherein the one servo wedge comprises a binary sequence having groups of no more and no fewer than two

consecutive logic 1's, the groups separated from each other by respective logic 0's (Col. 16, Lines 30-67. Tuttle teaches a group in which there is a group of two 0's and a group of two 1's.).

Regarding Claim 18, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 1. The combination further teach wherein the one servo wedge comprises a binary sequence having groups of no more and no fewer than two consecutive logic 1's, the groups separated from each other by respective logic 0's (Col. 16, Lines 30-67. Tuttle teaches a group in which there is a group of two 0's and a group of two 1's. Tuttle teaches that it uses two 0's to represent the binary value 0, and two 1's to represent the value –1, therefore, there can be at least two zeros of separation when representing –1 and 0 (For example 11000011= -1 0 0 -1).).

Regarding Claim 32, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 22. The combination further teach wherein the servo data comprises a preamble; wherein the servo channel is operable to generate a read signal that represents the servo data and to sample the read signal (Pat. No. 6, 108, 151; Fig. 2B); wherein the processor is operable to detect the servo data by detecting the preamble from the samples (Col. 4, Lines 57-60. It presents a channel that reads both servo and user data.); wherein the servo channel comprises an interpolator loop that coarsely adjusts respective phase angles the samples with respect to the read signal while the processor is detecting the preamble and that finely adjusts the phase angles of the samples a predetermined time after the processor detects the preamble (Pat. No. 6, 108, 151; Col. 21, Line 15 to Col. 22, Line 4); and an initial-phase circuit operable to calculate an initial phase angle between a sample and the read signal and to provide an initial

phase-angle adjustment to the interpolator loop while the interpolator loop is coarsely adjusting the phase angles of the samples (Pat. No. 6, 108, 151; Col. 21, Line 15 to Col. 22, Line 4).

Regarding Claim 39, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 38. The combination further teach wherein the first rotational speed is zero, or approximately zero (Pat. No. 6, 108, 151; Col. 15, Lines 13-15).

Regarding Claim 40, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 38. The combination further teach wherein the second rotational speed is a steady-state speed or is approximately a steady-state speed (Pat. No. 6, 108, 151; Col. 15, Lines 13-15. It is obviously to a person of ordinary skill in the art to know that in a disk after performing a spin-up operation, it eventually detects synchronously at a stable speed).

Regarding Claim 41, Sacks et al. and Tuttle et al. teach all the limitations of Claim 38. Tuttle et al. further teach wherein the circumferential position of the read head is unknown for the entire first time period (Pat. No. 6, 108, 151; Col. 15, Lines 15-30).

Regarding Claim 42, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 38. The combination further teach wherein the circumferential position of the read head is unknown for the entire first time period and for a second time period that follows and that is contiguous with the first time period (Pat. No. 6, 108, 151; Col. 15, Lines 15-30. Tuttle et al. that fir a time period the location of the head with respect to the disk is unknown.

Regarding Claim 43, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 38. The combination further teach wherein detecting the servo data

comprises detecting a preamble that composes the servo data (Pat. No. 6, 108, 151; Col. 15, Lines 15-30).

Regarding Claim 44, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 38. The combination further teach wherein determining the circumferential position of the read head comprises: recovering a data-location identifier from the servo data and determining the circumferential position of the read head from the data-location identifier (Pat. No. 6, 108, 151; Col. 15, Line 15 to Col. 16, Line 7. Tuttle et al. teach that the servo address mark indicates the position of the disk and it aids it in locating the other servo wedges.).

Regarding Claims 45 and 46, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 38. The combination further teach wherein detecting the servo data comprises accurately detecting a predetermined number of servo wedges before determining the circumferential position of the read head (Pat. No. 6, 108, 151; Col. 15, Line 15 to Col. 16, Line 7. Tuttle et al. teach that the servo address mark indicates the position of the disk and it aids it in locating other servo wedges.).

Regarding Claim 51, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 38. The combination further teach sampling the servo data and synchronizing the samples to the servo data by interpolating values of synchronized samples of the servo data from actual values of respective unsynchronized samples of the servo data (Pat. No. 6, 108, 151; Col. 22, Lines 5-55. Tuttle et al. teach that the interpolate circuit takes the samples of digital servo data and minimizes its phase, therefore eliminating its error and synchronizing the servo data.).

Regarding Claim 53, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 38. The combination further teach wherein detecting the servo data comprises detecting the servo data if and only if a predetermined number of consecutive samples of the servo data represent a preamble (Pat. No. 6, 108, 151; Col. 15, Lines 15-30. Tuttle et al. teach detecting a servo address mark which is found in the preamble.).

3. Claims 19, 36 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sacks et al. and Tuttle et al. as applied to claims 1 and 22, respectively above, and further in view of Patapoutian et al. (US Patent No. 5, 661, 760).

Regarding Claim 19, 36 and 57, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 1, 22 and 38, respectively. However, the combination does not explicitly teach wherein the servo wedge comprises a predetermined binary sequence having groups of no more and no fewer than a predetermined number of consecutive bits each having a first logic level, the groups separated from each other by respective bits having a second logic level; And the servo channel comprises a Viterbi detector that excludes state transitions that are excluded from the predetermined binary sequence. Patapoutian et al. teaches a first group of consecutive bits, the first group having first and second equally sized portions and representing a first logic level, the bits in the first portion each having a second logic level (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++-----++--++", having a first and second equally sized portion in the first group ("--++" and "++--") having a second logic level ("1") and a third logic level ("0")) and a Viterbi detector operable to

receive a signal that represents a binary sequence (Pat. No. 5, 661, 760; See Abstract). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention with the teaching of Patapoutian et al. in order to receive a binary sequence (Pat. No. 5, 661, 760; See Abstract).

4. Claims 20 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sacks et al. and Tuttle et al. as applied to claims 1 and 22 above, and further in view of Patapoutian et al. (US Patent No. 5, 661, 760) and Cloke et al. (US Patent No. 5, 822, 143).

Regarding Claims 20 and 37, the combination of Sacks et al. and Tuttle et al. teach all the limitations of Claims 1 and 22, respectively. The combination does not explicitly teach wherein the servo wedge comprises a predetermined binary sequence having groups of no more and no fewer than a predetermined number of consecutive bits each having a first logic level, the groups separated from each other by respective bits having a second logic level; And the servo channel comprises a Viterbi detector that excludes state transitions that are excluded from the predetermined binary sequence. Patapoutian et al. teaches a first group of consecutive bits, the first group having first and second equally sized portions and representing a first logic level, the bits in the first portion each having a second logic level (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoutian et al. teaches a ¼ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "1011" ("10" being a first logic level and "11" being a second logic level) will be encoded into "--++++----++--++", having a first and second equally sized portion in the first group ("--++" and "++--") having a second logic level ("1") and a third logic level ("0")) and a Viterbi detector operable to receive a signal that represents a binary sequence (Pat. No. 5, 661, 760; See Abstract). However, the

combination of Sacks et al., Tuttle et al. and Patapoutian et al. does not explicitly teach wherein calculating a respective path metric for each of no more than two possible states of the binary sequence and determining a surviving path from the calculated path metrics, the binary sequence lying along the surviving path. However, this feature is well known in the art as disclosed by Cloke et al., wherein it teaches a Viterbi detector that uses a trellis codes that search for a path metric (Pat. No. 5, 822, 143; See Fig. 1A and Col. 1, Lines 45-48, Lines 53-59 and Col. 1, Line 60 to Col. 2, Line 19). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention to use a path metric in order to effectively estimate the most likely sequence of symbols.

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sacks et al. and Tuttle et al. as applied to claim 1 above, and further in view of Ehrlich et al. (US Patent No. 6, 519, 107). The combination of Sacks et al. and Tuttle et al. teach all the limitations of Claim 1. However, the combination does not explicitly teach wherein the one servo wedge lacks an erase field. However, this feature is well known in the art as disclosed by Ehrlich, wherein it teaches servo wedge which lacks an erase field (Pat. No. 6, 519, 107; Col. 14, Lines 20-33). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify the combination's invention with the teaching of Ehrlich et al. in order to eliminate the erase field in order to provide positioning for the actuator head (Pat. No. 6, 519, 107; Col. 14, Lines 33-50).

Allowable Subject Matter

6. Claims 6, 7, 8, 9, 11, 12, 26, 27, 28, 30, 47, 48, 49, 50 and 52 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The reasons for indicating allowable subject matter are found in the Office Action dated January 24, 2005.

Response to Arguments

Applicant's arguments filed 12/27/05 of the After Final Action have been fully considered but they are not persuasive. The arguments are given the previous Office Action dated 01/20/06.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (571) 272-7561. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on (571) 272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gpr
05/12/06.

WAYNE YOUNG
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